ABSTRACT OF THE DISCLOSURE

A receive deserializer circuit which frames parallel data utilizes a skip-bit technique for aligning a predefined data reference pattern with a word clock. The receive deserializer circuit includes a sampling flip flop which receives serial data including a data reference pattern. The sampling flip flop samples and retimes the serial data to a recovered clock. A demultiplexer then deserializes the retimed serial data into a parallel data word which is timed to a word clock from a clock generator. A comparator makes comparisons of the parallel data word with a preset data reference pattern until a match results. A logic controller interprets whether the output of the comparator is a match and generates a shift pulse following each comparison which does not result in a match. The clock generator divides the recovered clock into eight phase clocks. One of the phase clocks is a word clock. Each time the clock generator receives a shift pulse from the logic controller, it disables all the phase clocks by one bit period. This results in a one bit shift in all the clocks and a one bit shift in the parallel data generated on word clock each time there is no match from the comparator. When a match occurs, no shift pulse is generated by the logic controller, and the predefined data reference pattern and subsequent data words received on word clock are properly framed.